

Appl. No. 09/832,167
Amtd. Dated June 13, 2005
Reply to Office Action of February 25, 2005

Attorney Docket No. 81784.0235
Customer No. 26021

REMARKS/ARGUMENTS:

Claims 1, 11, 20, 27, and 35 are amended. Claims 1-50 are pending in the application. Reexamination and reconsideration of the application, as amended, are respectfully requested.

Most of the independent claims are being extensively amended in order to distinguish patentably over the art. As mentioned in a recent exchange of phone messages between the undersigned and Examiner Kumar, the Examiner is requested to call the undersigned to discuss any further or different amendments that would be regarded as placing the application in condition for allowance.

The present invention relates to a method and circuit for driving a flat display device such as a liquid crystal display. The present invention also relates to a technique of generating a partial display on such a flat display device. (Applicant's specification, at p. 1, lines 5-8).

CLAIM REJECTIONS UNDER 35 U.S.C. §102

Claims 1, 5, 8-14, 16-23, 25-27, 29, 32-35, 37, and 40-50 stand rejected under 35 U.S.C. §102(e) as being anticipated by Yamazaki (US 2002/0175887 A1). The applicant respectfully traverses this rejection.

Independent claims 1, 11, 20, 27, and 35 are being amended to clarify that, during at least one frame period under a partial display mode, a partial display area having pixels of s rows by m columns which is a part of a display having pixels of n rows by m columns and an area having pixels of k rows by m columns which is a part of a background display area which is an area of the display of n rows by m columns different from the partial display area (i.e., the background display area has pixels of $(n-s)$ row by m columns) are selected in one frame period, arbitrary display data is written into the partial display area, and background data is written

into the area of k rows by m columns which is a part of the background display area.

In claims 1, 11, 20, 27, and 35 as previously presented, although selection of k rows by m columns within the background display area is described, there is no description that the area of k rows by m columns is “a part of” and not “the entirety” of the background display area. This is an important distinction as discussed below.

The Office states that “it is clear that Yamazaki teaches where data is written into selected pixels”. However, fundamentally, Yamazaki does not “need to select”, and, therefore, Yamazaki fails to teach or suggest active “selection” of an area which is called “non-display area” in Yamazaki.

Specifically, Yamazaki fails to teach or suggest a structure in which, during at least one frame period under a partial display mode, a partial display area having pixels of s rows by m columns which is a part of a display having pixels of n rows by m columns and an area having pixels of k rows by m columns which is a part of the background display area which is an area of the display of n rows by m columns different from the partial display area (i.e., the background display area has pixels of $(n-s)$ row by m columns) are selected in one frame period, arbitrary display data is written into the partial display area, and background data is written into the area of k rows by m columns which is a part of the background display area as described in the present invention.

In contrast, in Yamazaki, an area other than the partial display area, e.g., rows 1-40 in Yamazaki, is the partial display area and an area of rows 41-200 is a “non-display area”. Yamazaki explicitly states that a “non-selection voltage” is output to a selection line for selecting the switching element of each pixel in the “non-display area” so that the non-display area is always “not selected”.

Therefore, the present invention in which a “part” of the background display area is intentionally selected and “background data” is actively sequentially written

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into the background display area (through a plurality of frame periods) completely differs technically from Yamazaki in which there is no necessity or recognition of employing such a method.

When the background display area is not selected at all, the display quality in the area is degraded in that area. However, when background display data is written similarly as the partial display area, i.e., when the background display data is written while sequentially selecting all background display area within one frame period similar to the normal display mode, the problem of high power consumption cannot be solved.

Yamazaki discloses in Fig.23 and paragraphs [0245] – [0261], in addition to other places, a method of partial display in an active matrix LCD. However, as is clear from the description related to the operation of the active matrix LCD, in Yamazaki, the remaining area of the partial display area is an “area in which no display is achieved” and is switched off “at all times”. In particular, Yamazaki fails to disclose selection of a “part” of the non-display area along with the partial display area in one frame period. Furthermore, Yamazaki fails to teach or suggest the provision of a frame. As described, the present invention cannot be anticipated or rendered obvious over Yamazaki and there is no description in Yamazaki to motivate a person with ordinary skill in the art to make the present invention.

In light of the foregoing, Applicant respectfully submits that Yamazaki could not have anticipated or rendered obvious claims 1, 11, 20, 27, and 35, because Yamazaki fails to teach or suggest each and every claim limitation. Claims 2-5, 8-10, 12-14, 16-19, 21-23, 25, 26, 29, 32-34, 37, and 40-50 depend from either claim 1, 11, 20, 27, or 35 and therefore, cannot be anticipated or rendered obvious for at least the same reasons as these claims. Withdrawal of these rejections is thus respectfully requested.

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CLAIM REJECTIONS UNDER 35 U.S.C. §103:

Claims 6, 7, 15, 24, 30, 31, 38, and 39 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki. The Applicant respectfully traverses this rejection. Claims 6, 7, 15, 24, 30, 31, 38, and 39 depend from either claim 1, 11, 20, 27, or 35 and therefore, cannot be rendered obvious for the reasons discussed above. Withdrawal of these rejections is thus respectfully requested.

Claims 28 and 36 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki as applied to claims 27 and 35 above, and further in view of Irwin (US 6,057,820). The Applicant respectfully traverses this rejection.

Claims 28 and 36 depend from claims 27 and 35, respectively, and therefore, cannot be rendered obvious over Yamazaki for at least the same reasons discussed above. Irwin cannot remedy the defect of Yamazaki and is not relied upon by the Office for such. Instead, the Office cites Irwin for disclosing a frame counter for counting frames.

In light of the foregoing, Applicant respectfully submits that the cited references could not have rendered claims 28 and 36 obvious because the cited references fail to teach or suggest each and every claim limitation. Withdrawal of this rejection is thus respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

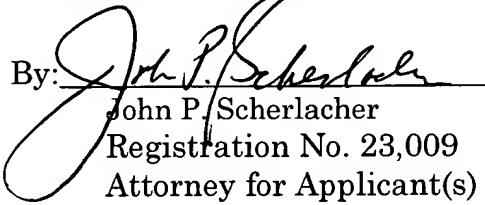
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If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: [MONTH #, #####]

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